A novel instrumentation amplifier with high tunable gain and CMRR for biomedical applications

Riyaz AHMAD[1,2]**, Amit Mahesh JOSHI**[1,*]**, Dharmendar BOOLCHANDANI**[1]

[1]Department of Electronics and Communication Engineering, Malaviya National Institute of Technology,
Jaipur, Rajasthan, India
[2]Department of Electronics Engineering, University Departments, Rajasthan Technical University,
Kota, Rajasthan, India

Abstract: A new design of current mode instrumentation amplifier (CMIA) with tunable gain and low voltage operation capability is proposed in this paper, which is suitable for biomedical signals processing, especially in electrocardiogram (ECG). It consists of a new design of current differencing transconductance amplifier (CDTA) and dual z copy CDTA (DZC-CDTA). The gain of the proposed CMIA is controlled by a MOS-based tunable resistor. The main advantage of the proposed CMIA is its high gain that can be tuned over a significant range with the help of two resistances. The performance of the proposed instrumentation amplifier is evaluated through simulation results on Cadence Virtuoso using SCL 180 nm CMOS technology. From simulation results gain, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), %THD and -3 dB bandwidth of proposed instrumentation amplifier are obtained as 55.09–81.12 dB, 90.42–116.5 dB, 97.3 dB ($+$PSRR), 114.2 dB ($-$PSRR), 1.5% and 9.5–165 kHz, respectively. The performance of the proposed design is also examined against PVT variations. The performance of proposed CMIA is compared with other existing designs available in the literature, which clearly shows the competency of the design. The post layout simulation results confirm the on-chip implementation feasibility.

Key words: Biomedical signal processing, instrumentation amplifiers, current differencing transconductance amplifier (CDTA), current mode instrumentation amplifier (CMIA), high gain amplifiers, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR)

1. Introduction

Traditionally, biomedical signals are acquired using sensing electrodes and amplified by using instrumentation amplifiers. These signals acquired from sensing elements need to be amplified to some higher range of value that is suitable for further processing like analog to digital conversion, display devices, and recorders. Instrumentation amplifier (IA) is an essential part for biopotential signal (i.e., ECG) detection. The bio potentials developed in the human body are of the order of few μV to a few mV [1]. To detect small range input signals in the presence of high flicker noise there is need of IA with low noise, high programmable differential gain, high CMRR and PSRR. The IA also put down the common mode signals like offset and noise.

IA is an important block of biomedical signal detecting systems, and, in this paper, current mode IA (CMIA) based on CDTA is proposed. CMIA is more appropriate because it does not require resistor matching

*Correspondence: amjoshi.ece@mnit.ac.in

to attain high CMRR in comparison to Op-Amp based voltage mode instrumentation amplifier (VMIA), which strongly depends upon matching of feedback resistors. Wilson [2] and Toumazou and Lidgey [3] have suggested a current-mode approach, which has a high CMRR without the need for matched resistors. Different CMRR enhancement techniques of current-mode instrumentation amplifiers are discussed and compared [4]. Another circuit in [5] is based on a current conveyor and operational amplifier that offers significant improvement in accuracy as compared with the basic current-mode instrumentation amplifier based on current conveyors only. In addition, there is low supply voltage requirement in CMIA as compared to VMIA. Several current mode signal processing active blocks have been realized to encounter the challenges and demands of the electronics industry [6, 7]. Current mode active building blocks like current conveyor (CC), current follower transconductance amplifier (CFTA), current backward transconductance amplifier (CBTA), CDTA etc. for analog signal processing were suggested and reviewed with some new proposals in the literature [8, 9]. CDTA [10] combines the advantages of second-generation current conveyor (CCII) [11] and OTA and has better performance compared to other current mode circuits like linearity, noise rejection capability, dynamic range, speed, and bandwidth.

In analog circuit design, there is often a large request for amplifiers with specific current performance for signal processing. It does not matter whether input is voltage or current, but the signal processing is performed in current domain. Instrumentation amplifiers are classified based on the manner in which input signal is processed and the output signal available [12]. Based on various current mode active building blocks (ABB) and the type of input and output signals, the CMIAs can be categorized in four main types as follows:

I. Voltage Input-Voltage Output (V-V) CMIA: The input and output signals are in voltage, but the signal processing is performed in current domain. High input impedance (ideally infinite) and low output impedance (ideally zero) are required for V-V CMIA.

II. Current Input-Current Output (I-I) CMIA: The input and output signals are currents, and the signal processing is performed in current domain; therefore, it can be called "pure" CMIA. The low input (ideally zero) and high output (ideally infinite) impedances are required for I-I CMIA.

III. Current Input-Voltage Output (I-V) CMIA: The input signal is in current, and the output signal is voltage. It has low input (ideally zero) and low output (ideally zero) impedances. This type is called trans-impedance (or trans-resistance) CMIA.

IV. Voltage Input-Current Output (V-I) CMIA: The input signal is in voltage, and the output signal is in current. It has high input (ideally infinite) and high output (ideally infinite) impedances. This type is called trans-conductance CMIA.

Out of four categories mentioned above, current input-current output (I-I) type CMIA is proposed in this paper. IA with low noise, high gain as well as high CMRR and PSRR with low power operation can be achieved if the design issues are addressed carefully. The literature survey on IA reveals that vast range of topologies are reported [13–39] . The current-mode instrumentation amplifier circuit is previously reported by Toumazou and Lidgey [3], and this was chosen as the basis for the development of second generation CMIA in which complex common-mode bootstrapping technique has been used to produce high CMRR [13]. The instrumentation amplifier using only current controlled conveyors (CCCIIs) is proposed in [14], providing low gain about 15-25 dB only. Complex structure and large device sizes are incorporated in [15]. An instrumentation amplifier circuit

is proposed by using current controlled current conveyors transconductance amplifiers (CCCCTAs) [16] with low gain and comparatively high power consumption. CMOS based instrumentation amplifiers use high supply voltage and provide low gain presented in [17] and comparatively low CMRR & PSRR reported in [18]. Another instrumentation amplifier based on op-amp in which power dissipation was very high for biomedical applications [19]. CMRR and PSRR were also low. The electronically tunable features of IA are based on current mode active building blocks that control some features such as gain, CMRR, input impedance, etc. This tunable capability of IA can be achieved by two methods. In the first method, parameters of IA are controlled by changing the bias voltage or current as reported in [20–24], while, in the second method, parameters are controlled by changing the value of electronically variable resistor as reported in [25–29]. The main drawback of the first method is the higher power dissipation due to variation in bias current in view of changing the gain, while the drawback of the second method is that the resistance value should be increased by means of bias voltage in order to achieve high gain.

After extensive investigation of references [13–39], it is observed that only few IA exist, which uses current-mode ABB having both input and output as current, i.e. I-I [24, 27–34] while V-V CMIA are given in literatures [16, 17, 30, 33, 35–38], V-I CMIA in [16, 17, 33] and I-V CMIA in [25, 33, 39]. The different current mode blocks based IA have been designed based on MOS transistors biased in subthreshold region [24], current operational amplifier (COA) [27, 28], CDTA [29], current feedback operational amplifier (CFOA) [30], MOS based configuration [31], current difference buffer amplifier (CDBA) [32], operation floating current conveyor (OFCC) [33], second generation current controlled conveyor (CCCII) [34].

The following observations have been made based on the literature survey of instrumentation amplifiers.

- The CMIA reported in [24], which operates in subthreshold region (is the only CMIA with both input and output signals being current and working in subthreshold), achieve high transconductance (g_m) and low power operation capability, has the issue of leakage current, larger device size, and limited input-output swing.

- To achieve high differential gain, a large resistor ratio is needed in [27, 30, 32–34], while [31] requires a large aspect ratio of transistors.

- Supply voltage and biasing current requirement are high in [29] to attain a significant range of gain. It is the only CMIA available in the literature that uses the CDTA block.

- Component matching is essential in [27, 30, 33] to increase the CMRR of IA.

It is deduced that most of topologies cited above are either operated in strong or subthreshold regime to attain the desired specification of IA. The techniques used and attractive benefit of the proposed CMIA can be observed as follows:

1. In this paper, a new design of CMIA is presented where almost all the MOS transistors are operating in moderate inversion to keep moderate device size in order to avoid parasitic and current leakage.

2. The proposed design provides the attractive benefit of increased gain compared to other existing design in the literature. To enhance the gain and CMRR of proposed design, the feedback arrangement is made such that it can be increased by setting fixed denominator resistor value and is further increased by changing the value of tunable resistor that appears in the numerator of the expression for gain of the proposed CMIA.

3. As low power operation capability is already supported in moderate inversion, it can be further improved by using g_m enhancement technique without increasing the bias current.

The paper is arranged in five sections including introduction. Section 2 discusses the characteristics and circuit diagram of both proposed DZC-CDTA and CMIA. However, g_m enhancement techniques suggested in [40, 41] were employed. Section 3 covers the nonideal performance of proposed CMIA. The simulation results, discussions, and performance comparisons with other existing CMIA are presented in Section 4, which also includes post layout simulation results. Finally, the paper is concluded in Section 5.

2. Proposed DZC-CDTA and proposed CMIA

In this section, the characteristics of proposed DZC-CDTA have been given, which is used in the design of proposed CMIA that is followed by the complete analysis of the proposed design.

2.1. Proposed DZC-CDTA for CMIA implementation

The basic working principle and symbolic notation of existing CDTA is given in [10]. Additional terminals z+ and z- can be provided to copy the current through the z terminal to add flexibility in the design. A novel CDTA is designed with an additional dual z copy unit. The symbol diagram of dual z copy CDTA (DZC-CDTA) is shown in Figure 1. The terminal equation for the DZC-CDTA is given in Eq. 1.
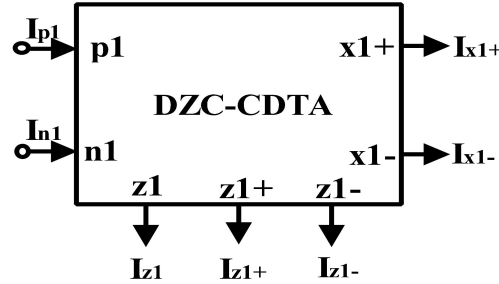

Figure 1. Symbol diagram of DZC-CDTA.

$$
\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_z+ \\ I_z- \\ I_x+ \\ I_x- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & -g_m & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_z+ \\ V_z- \\ V_x+ \\ V_x- \end{bmatrix} \tag{1}
$$

The DZC-CDTA circuit is designed using g_m/I$_D$ design methodology, and tradeoff in CMOS design [42, 43] is managed in such a way so that it is suitable to implement CMIA for biomedical application. The CMOS circuit implementation of proposed DZC-CDTA is shown in Figure 2(a) in which the first stage is CDU and is followed by ZCU. ZCU has been incorporated in the design to take freedom while designing the proposed CMIA. The last stage is the cross coupled transconductance amplifier. The DZC-CDTA without dual z copying unit (ZCU) can be considered as CDTA, and its CMOS implementation is shown in Figure 2(b). CDTA is

another block used in implementation of CMIA. The terminals current of DZC-CDTA and CDTA circuits are defined as per used in proposed CMIA. Some important features of proposed circuits are listed below:
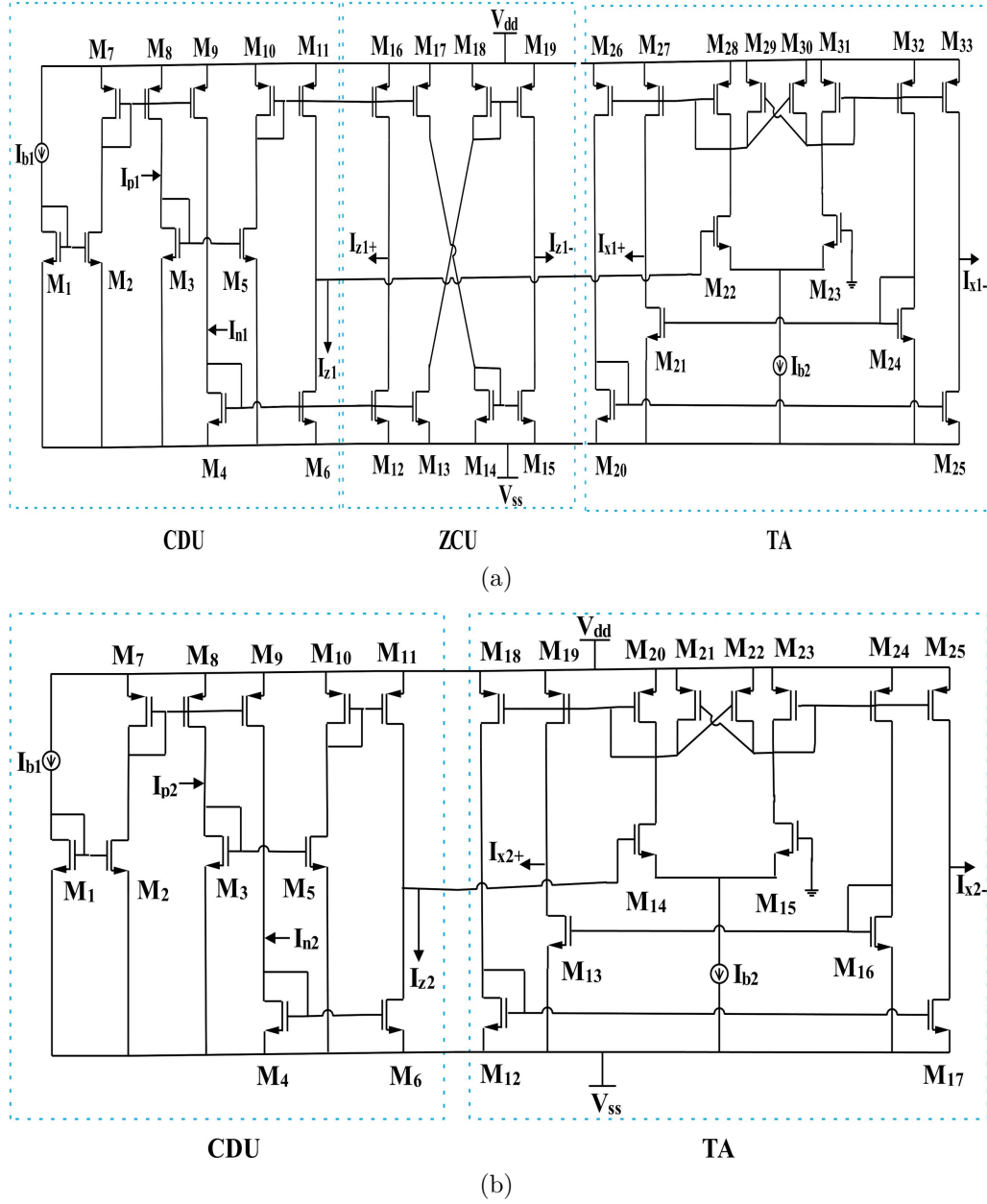

Figure 2. CMOS implementation of (a) DZC-CDTA, (b) CDTA.

- The upper and lower MOS transistor of CDU and ZCU is kept between moderate & low side of strong inversion (($g_m/I_D \approx 10$) to minimize the drain thermal noise.

- To minimize the input pair, input referred thermal noise current, the input device, i.e., TA is operated in between low side of weak inversion and moderate inversion ($g_m/I_D \approx 18$) for high g_m/I_D or g_m. This

helps the device to dominate the overall CDTA noise. Biomedical signals like ECG are very sensitive and noise may affect the performance of IA, since noise should be minimized.

- The high value of g_m/I_D is useful to minimize the loss of output range by minimizing their $V_{D,sat}$ value. The transconductance (g_m) of CDTA is increased by using cross coupled MOSFETs without increasing the bias current, which also pushes the design into the suitable range of low power biomedical applications.

- CMOS transconductance amplifier (TA) circuits use partial positive feedback for gain enhancement [40].The use of partial positive feedback using cross coupled MOSFETs not only increases the DC gain but also increases the unity gain bandwidth (UGB).

This increase in the gain and the bandwidth is a direct result of an increase in the effective transconductance of the input gain stage. As per the partial positive feedback principle given in [40], the effective transconductance (G_m)of given circuit can be directly derived from the DC transfer equation given below:

$$G_m = \frac{g_{m14}}{1 - \eta} \qquad (2)$$

The effective transconductance for the TA circuit shown in Figure 2(b) is enhanced by the factor of 1/ (1 - η). Where,

$$\eta = \frac{g_{m21}}{g_{m20}} \qquad (3)$$

By maintaining the same lengths for the active load transistors and the feedback transistors, η can be approximately written as

$$\eta = \frac{W_{21}}{W_{20}} \qquad (4)$$

If the ratio g_{m21}/g_{m20} is maintained close to unity, i.e., in the range of 0.9 to 0.99, a high (10 to 100 times) value of transconductance can be achieved. In conclusion, we say that, for a fixed power, partial positive feedback can be used to increase both the gain and the bandwidth of low power CMOS OTA designs. It is observed that partial positive feedback is a viable technique to increase the gain and the bandwidth of CMOS OTAs. Without any increase in power, approx a 20 dB increase in gain and a 5× improvement in bandwidth is feasible.

2.2. Analysis of proposed CMIA

The proposed structure of CMIA is shown in Figure 3. It employs one DZC-CDTA block, one CDTA block with MOS transistor dimensions similar to CDU and TA unit of DZC-CDTA, one resistor and one MOS based tunable resistor. The proposed CMIA can provide both noninverting and inverting output currents I_{out1} and I_{out2} via terminals z1+ and z1-, respectively. By applying KCL at both inputs of DZC-CDTA, we get

$$I_{z1} = I_{p1} - I_{n1} = I_{in+} + I_{x1+} + I_{x2+} - I_{in-} - I_{x1-} - I_{x2-} \qquad (5)$$

where

$$I_{x1+} = g_{m1}R_1I_{z1} = -I_{x1-} \qquad (6)$$

and

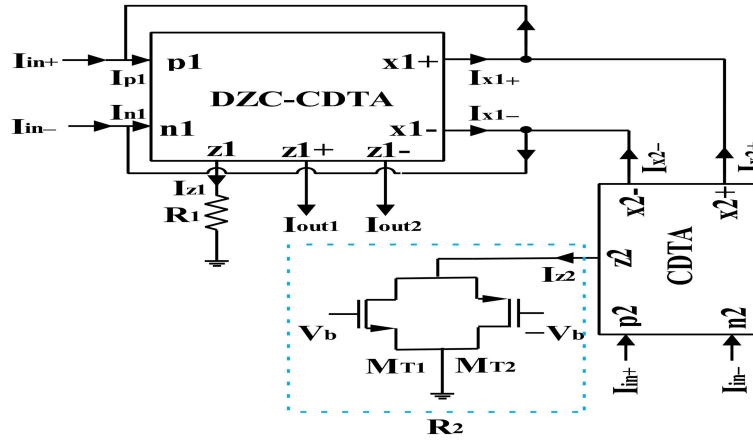$$I_{x2+} = g_{m2}R_2 I_{z2} = -I_{x2-} \tag{7}$$

Figure 3. CMIA implementation using CDTA and DZC-CDTA.

Substituting the values obtained in Eqs. 6, 7 into Eq. 5 gives

$$I_{z1} = I_{in+} - I_{in-} + 2g_{m1}R_1 I_{z1} + 2g_{m2}R_2 I_{z2} \tag{8}$$

Where, I_{z2} from Figure 3 is given as

$$I_{z2} = I_{p2} - I_{n2} = I_{in+} - I_{in-} \tag{9}$$

Substituting the value obtained in Eq. 9 into Eq. 8 gives

$$I_{z1} = (I_{in+} - I_{in-})(1 + 2g_{m2}R_2) + 2g_{m1}R_1 I_{z1} \tag{10}$$

Since,

$$I_{out1} = -I_{out2} = I_{z1} \tag{11}$$

Hence, the differential current gain of the proposed CMIA at noninverting and inverting output terminals is determined and given by Eqs. 12 & 13, respectively. (If $g_{m1} = g_{m2} = g_m$)

$$A_{d1} = \frac{I_{out1}}{I_{in+} - I_{in-}} = \frac{(1 + 2g_m R_2)}{(1 - 2g_m R_1)} \tag{12}$$

and

$$A_{d2} = \frac{I_{out2}}{I_{in+} - I_{in-}} = -\frac{(1 + 2g_m R_2)}{(1 - 2g_m R_1)} \tag{13}$$

From Eqs. 12 and 13, it may be noticed that by tuning the value of $2g_mR_1$ close to unity, the denominator becomes very small or close to zero; thus, very high values of differential current gain can be attained. Further improvement of the differential gain of proposed CMIA is possible by setting g_mR_2 to get higher values of gain with help of MOS based tunable resistor R_2. The proposed CMIA with tunable MOS resistor R_2 is shown in Figure 3.

The expression for tunable resistor using transmission gate transistors is given by

$$R_2 = \frac{1}{V_b(k_n + k_p) - (k_nV_{TH,n} + k_p|V_{TH,p}|)} \tag{14}$$

where V_b is gate bias voltage, $k_n = \mu_nC_{ox}W/L$ and $k_p = \mu_pC_{ox}W/L$ are device transconductance parameters of M_{T1} & M_{T2}, respectively, whereas $V_{TH,n}$ and $V_{TH,p}$ are threshold voltages. Thus, the differential current gain expression as a function of V_b can be derived by substituting the value obtained in Eq. 14 into Eq. 12 as

$$A_{d1} = \frac{[1 + 2g_m(\frac{1}{V_b(k_n + k_p) - (k_nV_{TH,n} + k_p|V_{TH,p}|)})]}{(1 - 2g_mR_1)} \tag{15}$$

Similarly, expression for A_{d2} can be determined by substituting the value obtained in Eq. 14 into Eq. 13. Since the proposed design provides the flexibility to achieve both non-inverting and inverting outputs, it is possible for the designer to achieve current inversion for further processing if required. From Eq. 5, it can also be observed that any common mode signal, whether it be in the form of dc offset, noise at input terminals, or a current bias in previous stages, will be automatically rejected by the proposed structure of CMIA due to differential input arrangement of CDTA.

3. Nonideal analysis of proposed CMIA

The CDTA with non-ideal characteristics mentioned in [41] is given in Figure 4. There are two types of nonidealities. First type of nonideality is tracking error at input terminals and error in transconductance. If these nonidealities are taken into consideration in analysis of proposed CMIA, the Eqs. 5 and 10 respectively become

$$I_{z1\_ni1} = \alpha_p(I_{in+} + I_{x1+} + I_{x2+}) - \alpha_n(I_{in-} - I_{x1-} - I_{x2-}) \tag{16}$$

and

$$I_{z1\_ni1} = (\alpha_pI_{in+} - \alpha_nI_{in-})[1 + (\alpha_p + \alpha_n)\beta_2g_{m2}R_2] + (\alpha_p + \alpha_n)\beta_1g_{m1}R_1I_{z1\_ni1} \tag{17}$$

where α_p and α_n are tracking error at input terminals and β_1 and β_2 are error in transconductance. Hence, the differential current gain A_{d1} and A_{d2} of Eqs. 12 and 13 gets amend to A_{d1_ni1} and A_{d2_ni1} respectively and A_{d1_ni1} is given as

$$A_{d1\_ni1} = \frac{I_{out1\_ni1}}{\alpha_pI_{in+} - \alpha_nI_{in-}} = \frac{[1 + (\alpha_p + \alpha_n)\beta g_mR_2]}{[1 - (\alpha_p + \alpha_n)\beta g_mR_1]} \tag{18}$$

Similarly, the expression for A_{d2_ni1} can be written. If $\alpha_p = \alpha_n = 1$ and $\beta_1 = \beta_2 = \beta = 1$, the nonideal gain
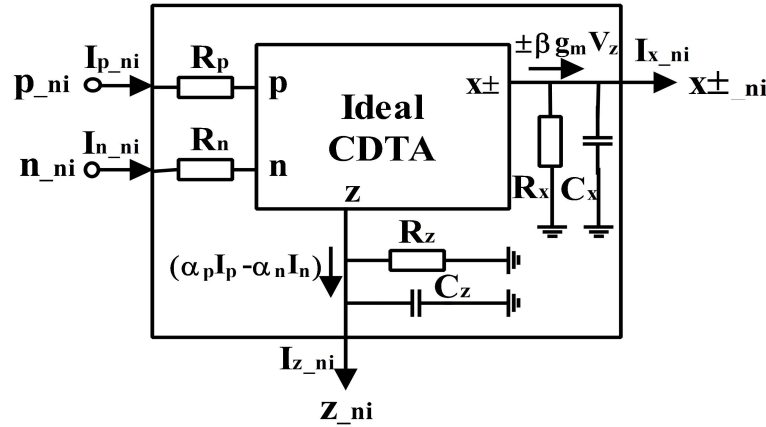
Figure 4. Symbol diagram of nonideal CDTA.

of Eqs. 18 reduces to the ideal case as shown by Eqs. 12.

To obtain the expressions of common mode current gain, we take $I_{in+} = I_{in-} = I_{com}$. The common mode gain with nonideality A_{c1_ni1} and A_{c2_ni1} at I_{out1} and I_{out2} can be determined as

$$A_{c1\_ni1} = \frac{(\alpha_p - \alpha_n)[1 + (\alpha_p + \alpha_n)\beta g_m R_2]}{[1 - (\alpha_p + \alpha_n)\beta g_m R_1]} = -A_{c2\_ni1} \tag{19}$$

So, the common mode rejection ratio (CMRR) of proposed CMIA can be derived as

$$CMRR = \frac{A_{d\_ni1}}{A_{c\_ni1}} = \frac{1}{(\alpha_p - \alpha_n)} \tag{20}$$

From Eq. 20, it can be observed that the CMRR of proposed CMIA approaches to infinity for $\alpha_p = \alpha_n$. Thus, it is possible to attain high values of CMRR.

Now let's consider the second type of nonideality, i.e., parasitic impedances and derive the expression of differential gain, common mode gain and CMRR of CMIA. The parasitic at terminal z1 appears in parallel with R_1, and at terminal z2 appears in parallel to R_2 and the differential current gains of Eqs. 12 get modified to (Generally, $R_{z1} >> R_1$ and $R_{z2} >> R_2$).

$$A_{d1\_ni2} = \frac{I_{out1\_ni2}}{I_{in+} - I_{in-}} = \frac{[1 + 2\beta g_m(R_2||\frac{1}{sC_{z2}})]}{[1 - 2\beta g_m(R_1||\frac{1}{sC_{z1}})]} \tag{21}$$

Similarly, the expression for A_{d2_ni2} can be written. Hence, considering the effect of parasitic, the CMRR also modifies to

$$CMRR = \frac{A_{d\_ni2}}{A_{c\_ni2}} = \frac{1}{(\alpha_p - \alpha_n)} \tag{22}$$

It can be observed from Eqs. 21 and 22, due to presence of parasitics, the differential current gain and CMRR of IA deviate from their ideal values, and this effect may be observable in the various simulation responses.

4. Simulation results

The performance of proposed CMIA has been evaluated by Cadence Virtuoso simulation software on Semiconductor Laboratory (SCL) 180 nm CMOS technology. The CMOS circuit implementation of DZC-CDTA and CDTA blocks used in proposed CMIA are shown in Figure 2(a) and 2(b), respectively. The dimensions of the MOS transistors of the DZC-CDTA and CDTA circuits are given in Table 1.

Table 1. Aspect ratio of transistor used in DZC-CDTA and CDTA blocks for implementation of CMIA.

DZC-CDTA		CDTA	
MOS Transistors	W/L(μm)	MOS Transistors	W/L(μm)
M_1-M_6, M_{12}-M_{15}, M_{20}-M_{21}, M_{24}-M_{25}	3.1/0.27	M_1-M_6, M_{12}-M_{13}, M_{16}-M_{17}	3.1/0.27
M_7-M_{11}, M_{16}-M_{19}, M_{26}-M_{33}	11.65/0.27	M_7-M_{11}, M_{18}-M_{25}	11.65/0.27
M_{22}-M_{23}	17.85/0.27	M_{14}-M_{15}	17.85/0.27

The power supply voltages are $V_{dd} = -V_{ss} = 0.9$ V for all simulation performed. The CDU bias current is set to be $I_{b1} = 50$ μA and TA unit bias current $I_{b2} = 100$ μA. The transconductance value of CDTA was 16.12 mS and the resistance R_1 was chosen 31 Ω to ensure g_mR_1 to be 0.5 to achieve high gain. These values of g_m and R_1 have been used for calculation until the end of this work. The aspect ratio of MOS transistor-based resistor R_2 is kept at $9.2\mu/0.27\mu$ to ensure linear region of operation the bias voltage $|Vb|$ is varied between 1.2-1.8 V. The high differential gain is observed in the range of 55.09-81.12 dB, CMRR ranges from 90.42 to 116.5, PSRR($+$) is 97.3 dB, PSRR($-$) is 114.2 dB and input referred input and output noises range from 62.5 pA to 31.5 nA@1 Hz-165 kHz and from 4.74 nA to 2.29 μA@1 Hz-165 kHz respectively. The percentage deviation in THD is approximately 1.5%. The achieved results satisfy the requirements of instrumentation amplifiers for biomedical applications.

4.1. DC analysis

The DC response plot for the proposed CMIA is shown in Figure 5. The DC response for various values of $|Vb|$ has been analyzed. The input current is varying from -100 nA to 100 nA. The linear performance is evaluated for the $|Vb|$ varying from 1.4V to 1.8 V in steps of 0.1 V.

4.2. Transient analysis

The transient response plot is shown in Figure 6. To test the output with respect to time an input current of amplitude 50 nA and frequency 1 kHz is applied. The bias voltage $|Vb|$ is varied from 1.3 V to 1.8 V in steps of 0.1 V. It is observed that the waveforms are purely sinusoidal in nature with negligible offset.

4.3. AC analysis

The AC response of proposed CMIA is analysed and an AC signal of 50 nA magnitude is applied for analysis. The differential gain as given by Eq. 12 of proposed CMIA should attain infinity when the value g_mR_1 is 0.5. From the expression given in Eq. 12 it is observed that differential gain is also proportional to g_mR_2. Hence it provides further enhancement in the magnitude of the differential gain. The MOS based resistor R_2 is used for tuning the gain. The differential gain for different values of $|Vb|$ varying from 1.2 V to 1.8 V in steps of 0.1
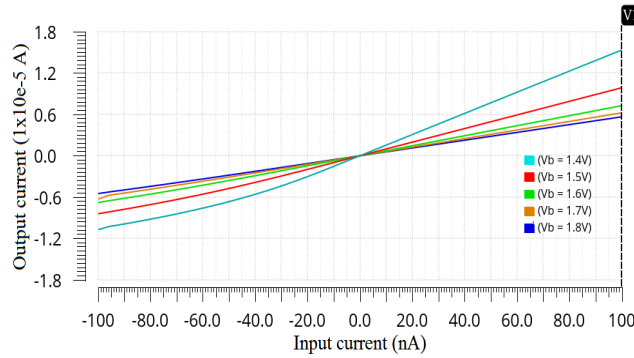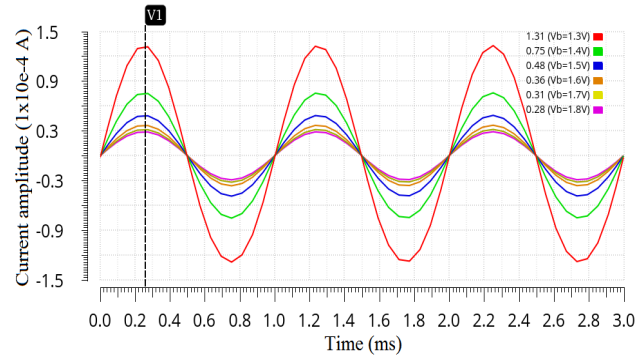
Figure 5. DC response

Figure 6. Transient response

V is shown in Figure 7(a). It is observed that the maximum value of differential gain is 81.12 dB with -3dB bandwidth of 9.5 kHz where as the minimum differential gain is 55.09 dB with -3dB bandwidth of 165 kHz.

The important feature of IA, the common mode rejection ratio (CMRR) for different values of $|Vb|$ from 1.2 V to 1.8 V in steps of 0.1 V is shown in Figure 7(b). It is observed that CMRR is in the range from 90.42 dB to 116.5 dB, which is suitable for biomedical signal processing and higher than the minimum CMRR specified, i.e., 89 dB by the AAMI (Association for the Advancement of Medical Instrumentation) for standard ECG.
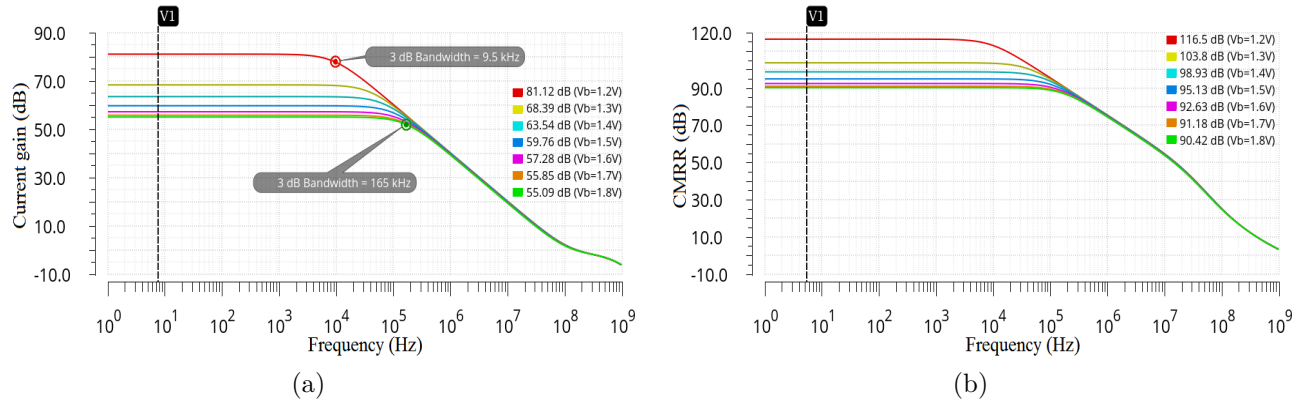

Figure 7. AC response (a) differential gain, (b) CMRR.

4.4. Noise analysis

As in the biomedical applications, signal frequencies are low, the IA should have good noise immunity at input. This feature of the proposed design is tested via noise analysis performance. Generally, two types of noises have main concer: first is thermal noise and second is flicker noise, which is more important especially at low frequency applications. From Eq. 5 of revised manuscript, it can also be observed that any common mode signal, whether it is in the form of dc offset, noise at input terminals or a current bias in previous stages will be automatically rejected by the proposed structure of CMIA due to differential input arrangement of CDTA. Hence, we can say that the major role in noise contribution is due to the input device i.e., TA unit. To minimize the input pair, input referred thermal noise current, the input devices of TA is operated in between low side of weak inversion and moderate inversion ($g_m/I_D \approx 18$) for high g_m/I_D or g_m. This helps the device to dominate the overall CDTA noise.

Let's first discuss the thermal noise contribution of TA. The TA part of CDTA is shown in Figure 2(b). The TA input-referred thermal-noise voltage, power spectral density (PSD) is given by

$$S_{VIN}(thermal) = 4kT[2 \times \frac{(n\Gamma)_{14}}{g_{m14}} + 2 \times \frac{(n\Gamma)_{12}g_{m12}}{g^2_{m14}} + 2 \times \frac{(n\Gamma)_{16}g_{m16}}{g^2_{m14}} + 3 \times \frac{(n\Gamma)_{20}g_{m20}}{g^2_{m14}} + 3 \times \frac{(n\Gamma)_{23}g_{m23}}{g^2_{m14}}] \quad (23)$$

gm14, gm12, gm16, gm20, and gm23 are transconductances for the transistors M14 and M15 input differential pair, non-input transistors M12 and M17, M13 and M16, M18, M19 and M20 and M23, M24 and M25 current-mirror devices, respectively. $(n\Gamma)_{14}$, $(n\Gamma)_{12}$, $(n\Gamma)_{16}$, $(n\Gamma)_{20}$ and $(n\Gamma)_{23}$ are the products of the substrate factor, n, and thermal-noise factor, Γ. The "2 and 3" appear in the noise expression because pair devices are used throughout the signal path, doubling or tripling the noise PSD associated with single devices. The first term in Eq. 23 corresponds to the gate-referred thermal-noise voltage PSD of the input differential-pair devices. The second, third, fourthand fifth terms correspond to the drain-referred thermal-noise voltage PSD of the non-input, current-mirror devices, with each term divided by the square of the input pair transconductance, g^2_{m14}. For TA, input-referred thermal-noise voltage is minimized by operating input devices at low inversion coefficients (IC14 = IC15, in weak or moderate inversion for high gm/ID and gm. The relation between gm and IC is given in [42] as,

$$g_m = \frac{I_D}{nV_T\sqrt{(IC + 0.5\sqrt{IC} + 1)}} \quad (24)$$

It is observed from the Eq. 23 that high gm of input devices M14 and M15 reduces the thermal noise as it is inversely proportional in all factors of noise. Hence, gm enhancement technique is also useful to reduce the thermal noise contribution of TA as the effective gm value increases, while non-input devices operate at moderate inversion coefficients in moderate inversion for moderate gm/ID and gm.

Now let's determine the input referred flicker-noise voltage PSD for the TA shown in Figure 2(b), and the expression can be written as

$$S_{VIN}(flicker) = 4kT[2 \times \frac{K_{F14}}{(WL)_{14}f^{AF14}} + 2 \times \frac{K_{F12}}{(WL)_{12}f^{AF12}}(\frac{g_{m12}}{g_{m14}})^2 + 2 \times \frac{K_{F16}}{(WL)_{16}f^{AF16}}(\frac{g_{m16}}{g_{m14}})^2$$
$$+ 3 \times \frac{K_{F20}}{(WL)_{20}f^{AF20}}(\frac{g_{m20}}{g_{m14}})^2 + 3 \times \frac{K_{F23}}{(WL)_{23}f^{AF23}}(\frac{g_{m23}}{g_{m14}})^2] \quad (25)$$

KF14, KF12, KF16, KF20 and KF23 are flicker-noise factors for the M14 and M15 input differential pair, non-input M12 and M17, M13 and M16, M18, M19 and M20 and M23, M24 and M25 current-mirror devices, respectively. AF14, AF12, AF16, AF20 and AF23 are the flicker-noise slopes, and (WL)14, (WL)12, (WL)16, (WL)20 and (WL)23 are the gate areas in µm^2 for these devices. As in the preceding thermal noise analysis, "2 and 3" appear in the noise expression because pair devices are used throughout the signal path, doubling and tripling the noise PSD associated with single devices. The first term in Eq. 24 corresponds to the gate-referred flicker-noise voltage PSD of the input differential-pair devices. The second, third, fourth, and fifth terms correspond to the drain-referred flicker-noise voltage PSD of the non-input, current-mirror devices. This is the gate-referred flicker-noise voltage PSD of these devices multiplied by the square of their transconductances. Each noninput device term is divided by the square of the input pair transconductance, g^2_{m14}. For TA, input-referred flicker-noise voltage is minimized by operating input devices at low inversion coefficients (IC14 = IC15) and comparatively long channel lengths (L14 = L15), which maximizes their gate area. Additionally, gm/ID

and g$_m$ are high at low inversion coefficients in weak or moderate inversion and also enhanced by g$_m$ boosting technique, helping input devices to dominate the noise. In addition to minimizing the flicker noise of input devices, minimizing overall TA flicker noise requires minimizing the noise of noninput devices.

The responses for input referred input noise and input referred output noise are exhibited in Figure 8(a) and 8(b) respectively. Their respective values range from 62.5 pA to 31.5 nA@1 Hz-165 kHz and from 4.74 nA to 2.29 μA@1 Hz-165 kHz. The noise is measured for the whole operating band of frequency of the proposed CMIA.
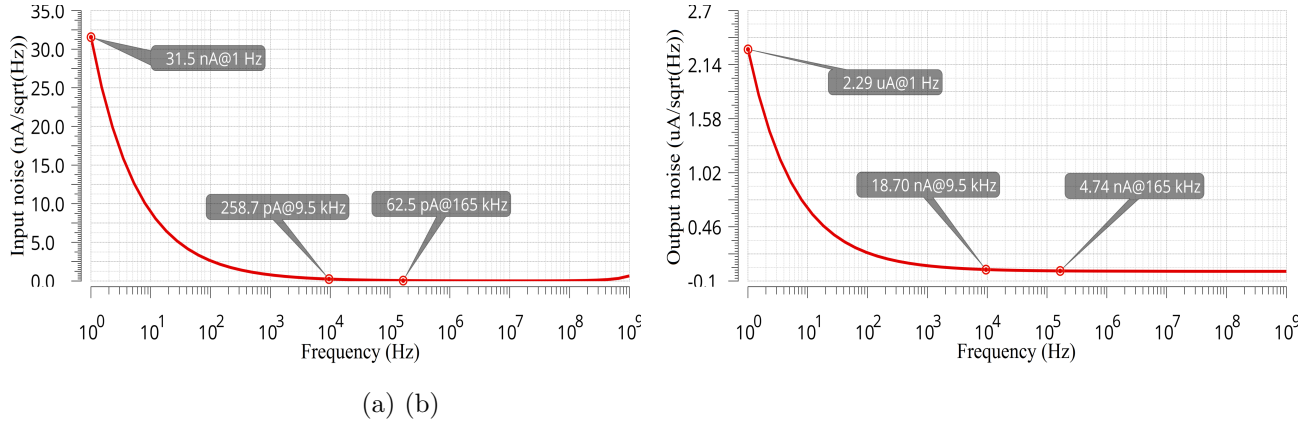

(a) (b)

Figure 8. Noise analysis (a) Input referred input noise (b) Input referred output noise

4.5. Performance (PVT) analysis

PVT analysis has been performed to understand if there are any variations in the transient characteristic of proposed CMIA. For the process variation, slow-slow, fast-slow, typical, slow-fast, fast-fast are analysed and the respective amplitude of currents are 1.33×10^{-4} A, 1.19×10^{-4} A. 1.31×10^{-4} A, 1.62×10^{-4} A and 1.65×10^{-4} A. By varying supply voltage $\pm 5\%$, the currents range from 1.26×10^{-4} A to 1.36×10^{-4} A. The temperature varies from -40 °C to 100 °C with intermediate temperature at -10 °C, 30 °C and 70 °C, output current ranges from 1.11×10^{-4} A to 1.43×10^{-4} A. The simulation results of PVT analysis are shown in Figure 9(a), 9(b), 9(c).

4.6. xf and THD analysis

The xf analysis was performed to test the proposed CMIA noises and disturbance rejection against power supply variations. The power supply rejection ratio, PSRR(+) and PSRR($-$) were observed as 97.3 dB and 114.2 dB respectively. Also to understand the effect of distortion on output current of proposed CMIA, total % harmonic distortion (THD) was plotted at a fixed fundamental frequency of 150 Hz and variation of %THD for different values of Vb was observed. It was found that the %THD variation is in satisfactory range with approximately 1.5% deviation.

Various analysis have been performed to verify the performance parameters of proposed CMIA. Summary of performance parameters of proposed CMIA is shown in Table 2.

4.7. Post layout simulations

To observe the effect of parasitics on the proposed circuit of CMIA, the layout has been drawn. The layout of proposed CMIA is shown in Figure 10. The area of proposed design is 4412 (80.66×54.70) μm^2 and to
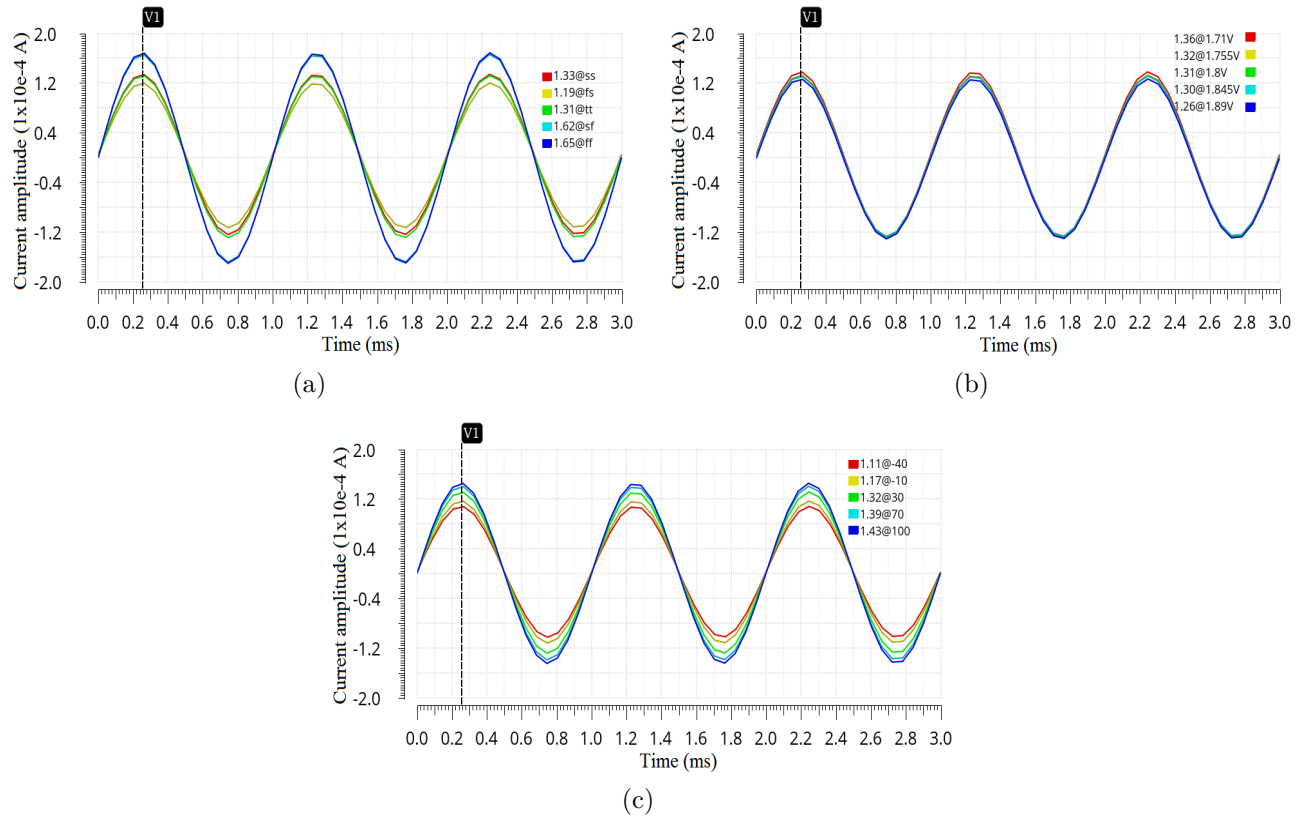
(a)

(b)

(c)

Figure 9. PVT analysis (a) process variation (b) voltage variation (c) temperature variation

Table 2. Summary of performance parameter of proposed CMIA

Parameters	Simulated values
Transistor process, Power supply	SCL CMOS, 0.18 μm, $\pm$0.9 V
Gain	55.09-81.12 dB @V$_b$ from 1.2 to 1.8 V
CMRR	90.42-116.5 dB @V$_b$ from 1.2 to 1.8 V
-3 dB Bandwidth	9.5 kHz@ gain 55.09 dB and 165 kHz@ gain 81.12 dB
PSRR($+$), PSRR($-$)	97.3 dB, 114.2 dB
Input and output reffered noise	62.5 pA-31.5 nA@1 Hz-165 kHz and 4.74 nA-2.29 μA@1 Hz-165 kHz
Power dissipation	1.44 mW

compare the schematic simulation results, the post layout simulations have been performed.

Pre and post layout simulations are compared for only one value of $|Vb|$. From Figure 11(a), it is clear that the DC output current of proposed CMIA obtained in pre-layout is close to the post-layout simulation result for $|Vb| = 1.5$ V. The pre and post-layout transient response plot is shown in Figure 11(b), for $|Vb| = 1.3$ V. An input current of amplitude 50 nA and frequency 1 kHz is applied. The variation observed between pre and post layout results is approximately 6%. The effects of parasitics can be clearly observed from the pre and post-layout AC responses of differential gain for $|Vb| = 1.3$ V, as shown in Figure 11(c). The differential current gain reduces from 68.39 dB to 65.73 dB. Still these values are satisfying the requirement for biomedical

applications. Also, the maximum deviation of theoretical and simulated gain evaluated for proposed CMIA was observed as 1.99 dB.
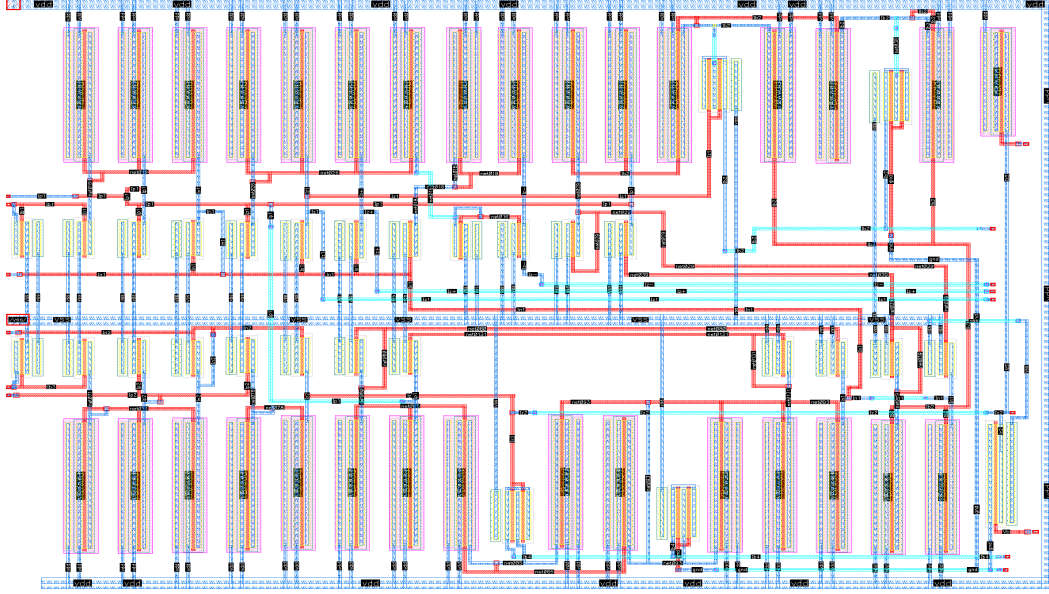

Figure 10. Layout of Proposed CMIA

4.8. Monte Carlo analysis

The robustness of the proposed CMIA has been verified by Monte Carlo analysis. Monte Carlo simulations are carried out with random distribution (no. of samples = 1000) and 5% mismatch. Monte Carlo analysis is performed for 1000 runs and Gaussian random variations has been given for changing the differential gain in dB and common mode gain in dB at bias voltage $|Vb|$ of 1.3 V. From Figure 12(a) and 12(b), the mismatch effect can be observed on differential gain and common mode gain. Also, the mismatch effect can be observed on CMRR (differential gain$-$common mode gain). It is observed that mean and standard deviation are not much deviated from value of differential gain (68.39 dB) and CMRR $[68.39 - (-35.41) = 103.8$ dB] at $|Vb|$ of 1.3 V. Therefore, the designs of proposed CMIA are robust and found to be satisfactory even after the change in device parameters. The mean, standard deviations values for differential and common mode gain are 67.55 dB, 0.945 dB and -33.13 dB, 0.65 dB, respectively

4.9. Comparison with existing literatures

The performance of proposed CMIA is compared with performance of those circuits that are already published in the literature as shown in Table 3. As it can be observed from the results that the proposed CMIA is the first one among the literature, which is implemented using MOS transistors operated in moderate inversion region, it also provides the highest gain with respect to already published designs as given in Table 3. The literature [16, 29, 33, 34] offers comparatively good CMRR but power consumption is high and comparatively low gain obtained. It can be observed that in [20, 24, 27] gain as well as CMRR are low.The literature [17, 36] shows a good CMRR but poor gain and high power supply requirement. Proposed design provides highest gain, good
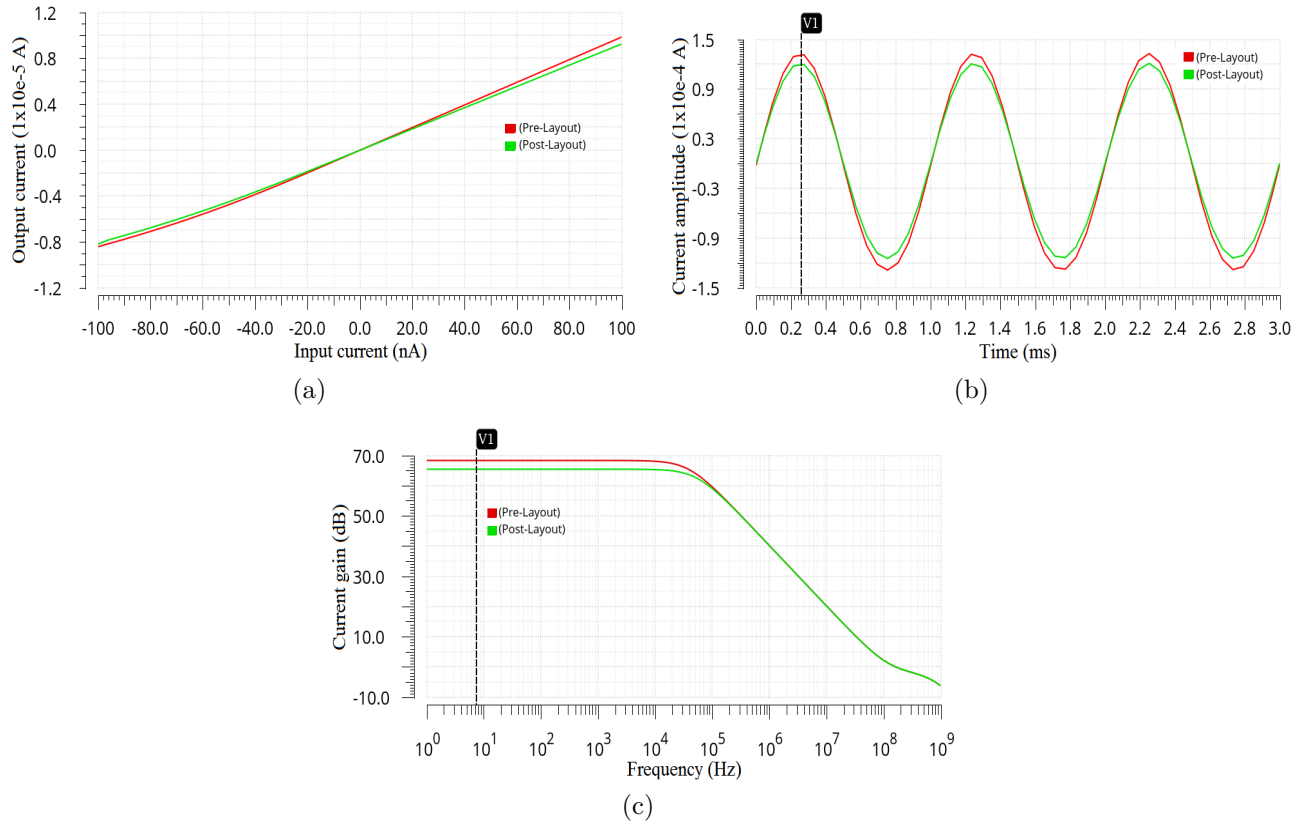
(a)

(b)

(c)

Figure 11. Post-Layout responses (a) DC (b) Transient (c) AC (Differential Gain)
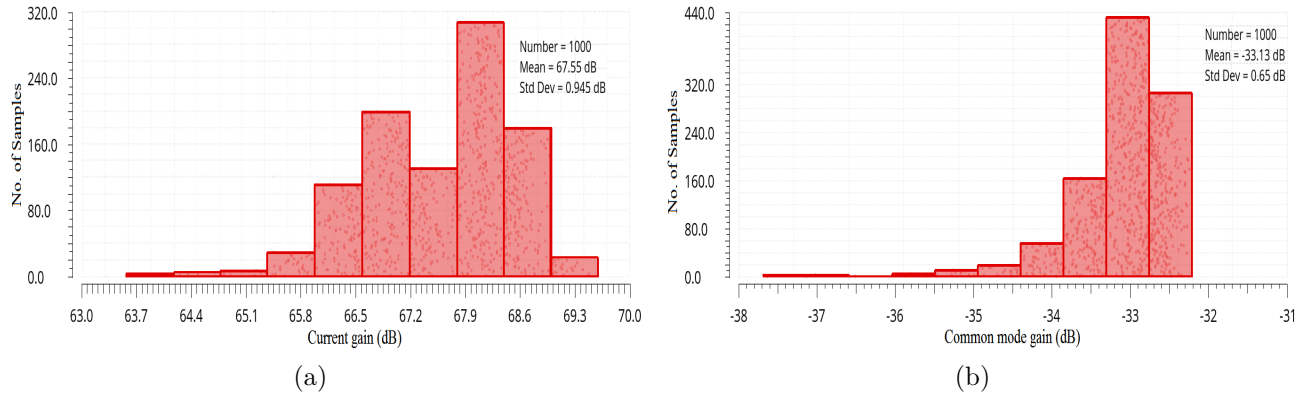

(a)

(b)

Figure 12. Monte Carlo simulations.(a) differential gain, (b) common mode gain.

CMRR, high PSRR, comparatively low power consumption and suitable range of bandwidth (9.5-165 kHz) for biomedical applications. The focused design parameters of proposed CMIA, high gain, high CMRR and low power consumption are competitive in comparison to the literatures compared.

Table 3. The performance results comparison of proposed CMIA

Ref.	Process (μm)	ABB Elements	Input-Output Signals	Region of operation	Gain (dB)	CMRR (dB)	PSRR (dB)	Power supply(V)	Power dissipation	−3dB BW (MHz)
[16]	0.35	CCCCTA	(V-V, V-I)	Strong	13-17	94	NA	± 1.5	4.43 mW	83.75
[17]	0.35	CMOS CC	(V-V,V-I)	Strong	16.7-28.7	142	NA	± 3.3	0.519 mW	70
[36]	0.35	DVCC	(V-V)	Strong	26	107	NA	± 1.65	0.528 mW	0.0125
[20]	0.18	ECCII	(I-I)	Strong	0-27	42	NA	± 0.9	0.95-1.73 mW	68
[24]	0.35	CMOS CM	(I-I)	Sub-threshold	20-40	44.4-48.9	146	± 0.75	0.07-0.39 μW	0.007
[33]a	NA	OFCC	(I-I)	Strong	21-36	55	NA	± 1.5	5.04 mW	20.85
[33]b	NA	OFCC	(I-I)	Strong	9-23	85	NA	± 1.5	3.99 mW	20
[34]	0.35	CCCII	(I-I)	NA	9.6-29.8	201.8-210.9	NA	± 0.75	3.5-7.7 mW	86.1-91.9
[27]	0.18	COA	(I-I)	Strong	6.9-25	36-54.2	NA	± 0.9	0.76 mW	1.8-19.35
[29]	0.18	CDTA	(I-I)	Strong	53.7-64	230-350	NA	± 1.8	6.84 mW	0.9-4.8
This Work	0.18	CDTA	(I-I)	Moderate	55-81	90.4-116.5	97.3*, 114.2**	± 0.9	1.44 mW	0.0095-0.165

ABB-Active Building Block, *PSRR(+), **PSRR(−)

The proposed CMIA was realized by using discrete components also. The CDTA implementation using second generation current conveyor (CCII+) and dual output operational transconductance amplifier (DO-OTA) given in [10], were used as basis for realization of proposed CMIA structure. The ICs, AD844 and LM13700 were used for implementation of CCII+ and dual output OTA respectively. The CCII+ was implemented using a single IC, AD844 and the DO-OTA was implemented using IC, LM13700 [45]. As in the proposed CMIA structure DZC-CDTA is also used, the CCII− were used to generate inverse of z terminal current. The CCII− were implemented using two IC, AD844. By using the structures explained as above, the complete experimental setup was created for the proposed CMIA. The CMRR and offset values were not good due to excessive wiring and area of prototyping board, but the implemented circuit provides clear output as expected.

5. Conclusion

In this work, a new design of CDTA based CMIA is proposed. The performance results have been verified in Cadence virtuoso using SCL 180 nm CMOS technology. The various simulations are performed to support the proposed design and results are well-suited for biomedical application. A very high electronically tunable differential gain 55.09-81.12 dB is achieved, hence useful to detect even if there are very small amplitude biopotential signals present. Some complexity in CMIA structure can be observed in order to achieve the desired output.To add further scope in design of the proposed CMIA, both resistors may be used as MOS transistor based electronically tunable resistors . Apart from biomedical applications, there is future scope of CDTA based CMIA in other fields like high speed signal conditioning, data acquisition, audio and video application, monitor and control electronics etc. Post layout simulations confirm the feasibility of on-chip fabrication.

Acknowledgements

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